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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,058	04/27/2005	**Mihai Adrian Tiberiu Sanduleanu**	NL02 1079 US	9258

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EXAMINER	
PEREZ, JAMES M	
ART UNIT	**PAPER NUMBER**
2611	

NOTIFICATION DATE	DELIVERY MODE
02/25/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/533,058	SANDULEANU, MIHAI ADRIAN TIBERIU	
	Examiner	Art Unit	
	JAMES M. PEREZ	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 5-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2,5,6,8 and 9* is/are allowed.

6)☒ Claim(s) *7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/24/2008* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to the Request for Continued Examination filed on 1/6/2010. Currently, claims 1-2 and 5-9 are pending.

1. The indicated allowability of claim 7 is withdrawn in view of the newly discovered reference(s) Tamaki et al. (cited in the IDS filed on 1/6/2010). Rejections based on the newly cited reference(s) follow.

2. Applicant is advised that the Notice of Allowance mailed is vacated. If the issue fee has already been paid, applicant may request a refund or request that the fee be credited to a deposit account. However, applicant may wait until the application is either found allowable or held abandoned. If allowed, upon receipt of a new Notice of Allowance, applicant may request that the previously submitted issue fee be applied. If abandoned, applicant may request refund or credit to a specified Deposit Account.

Drawings

3. The Drawings are objected to because for the following informalities:

(1) Figure 1 is objected to as failing to comply with 37 CFR 1.84(n) because the graphical drawing symbols (L1, L2, and D) do not use conventional symbols to represent the cited elements. Figure 5 shows appropriate graphical drawing symbols for low-pass filter and the examiner suggests inserting the wording “d/dt” into the graphical box corresponding to element D. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference

character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities:

(1) The description of the figure 1 (instant specification: page 1, line 14 through page 2, line 3) contains various terminology which is not consistent with the labeling of the elements of figure 1. Examples of such inconsistencies are "input signal INP" and "derivation circuit D1".

(2) The instant specification does not separate the specification sections using section headings as required by 37 CFR 1.77(c). See MPEP § 608.01(a).

(3) Appropriate correction is required.

Response to Arguments

5. Applicant's arguments with respect to claim 7 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moser (USPN 6,853,696) in view of Sudjian (US 7,409,027) further in view of Tamaki et al. (USPN 6,218,907: herein referenced as Tamaki).

With regards to claim 7, Moser teaches a Phase Locked Loop (PLL) for synchronization with an incoming data signal (fig. 1: col. 1, lines 25-30 and col. 6, lines 12-41: where the clock recovery unit achieves a phase and frequency lock-in condition with the input signal (col. 2, lines 25-35) and therefore is a type of PLL) comprising:

a voltage controlled oscillator generating mutually quadrature phase shifted signals (figs. 1 and 4: elements VCO, ICK and QCK).

a frequency detector (figs. 1 and 2: element 10: col. 5, lines 28-34: note that fig. 2 is the circuit diagram schematic illustration of the frequency detector usable in the embodiment shown in fig. 1) including an unbalanced quadricorrelator (fig. 2: col. 7, lines 8-15: note the digital frequency detector in its entirety is an unbalance quadricorrelator, where an unbalance quadricorrelator is a type of frequency detector), the quadricorrelator (fig. 2: col. 7, lines 8-15) comprising:

a first pair of clocked bi-stable circuits (fig. 2: elements 22, 30a, and 30b: col. 7, lines 29-49) coupled to the first multiplexer (fig. 2: elements 22 and 32: col. 7, lines 29-49), and a second pair of clocked bi-stable circuits (fig. 2: elements 20, 26a, and 26b: col. 7, lines 29-49) coupled to the second multiplexer (fig. 2: elements 20 and 28: col. 7, lines 29-49), which first and second pairs (fig. 2: elements 20 and 22) are supplied by mutually quadrature phase shifted signals (fig. 2: elements 20 and 22, which respectively use quadrature clock signals ICK and QCK) respectively to provide the first signal (fig. 2: FQ2) and the second signal (fig. 2: FQ1) indicative for a phase difference between the incoming signal and mutually quadrature phase shifted signals (fig. 2: elements 20 and 22: col. 7, lines 29-49: wherein the output signals (labeled FQ1 and FQ2) from the frequency detector give correlative information about a quadrature phase relationship (col. 8, lines 42-52), which is similar to output signals 'PI' and 'PQ' in figure 2 of the instant application);

a phase detector (fig. 2: elements 34a and 34b: col. 7, lines 50-63: wherein the examiner interprets said D flip-flops to be phase detector since elements 34a and 34b are clocked and input FQ1 and FQ2 respectively, where FQ1 and FQ2 give correlative information about a quadrature phase relationship (col. 8, lines 42-52)) controlled by the first signal provided by the first multiplexer (fig. 2: col. 7, lines 50-63: FQ2) and by the second signal provided by the second multiplexer (fig. 2: col. 7, lines 50-63: FQ2).

Moser does not explicitly teach two Limitations: Limitation 1) a frequency detector including double edge clock bi-stable circuits and a phase detector controlled by a first

signal pair provided by the first multiplexer and by a second signal pair provided by the second multiplexer (emphasis added); and Limitation 2) a first low-pass filter; a second low-pass filter; an adder; a first charge pump for inputting a coarse control input for the voltage controlled oscillator using a frequency error signal produced by the quadricorrelator and coupled to the first low-pass filter and to the adder; a second charge pump; and a further phase detector; wherein a fine control input is controlled by a signal provided by the further phase detector coupled to the second charge pump coupled to the second low-pass filter.

Limitation 1)

Sudjian teaches adapting D flip-flops (figs. 3 and 4: elements 22a-22b and 32a-32b) and multiplexers (figs. 3 and 4: elements 22a-22b and 34) to be compatible with differential incoming data signals (fig. 3: signal DATA: col. 5, lines 54-65) and differential quadrature clock signals (fig. 3: elements VCO_0 and VCO_90: col. 5, lines 54-65).

One of ordinary skill in the art at the time of the invention would clearly recognize the benefits of modifying the quadricorrelator of Moser to with the teachings and differential circuitry of Sudjian to yield the predictable benefits and results of implementing frequency detection (using a quadricorrelator) on a differential data signal as opposed to a single-end signal. Specifically, it would have been obvious to modify the known frequency detector circuitry (Moser elements 20 and 22 which are with in the quadricorrelator) with the known differential D flip-flops and differential multiplexers of Sudjian in order to perform similar functions on a differential input data signal and differential quadrature clocking signal to generate differential error signals (where FQ1

and FQ2 are originally single-end signals), where the modified FQ2 and FQ1 are the claimed first and second signal pair, respectively, and the differential D flip-flop pairs clock by differential quadrature clock signal are obviously double edge clock bi-stable circuits, and the relationship between the phase detector (Moser: fig. 2: elements 34a and 34b) and signals FQ1 and FQ2 was previously addressed. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the quadricorrelator (frequency detector) of Moser to with the teachings and differential circuitry of Sudjian to yield the predictable benefits and results of implementing frequency detection (using a quadricorrelator) on a differential data signal as stated above.

Limitation 2)

Tamaki teaches a Phase Locked Loop for synchronization with an incoming data signal, comprising:

a voltage controlled oscillator generating mutually quadrature phase shifted signals (figs. 1 and 4: element 31: VCO, CLK, and SCK: col. 4, line 64 through col. 5, line 2: note the 90 degree phase difference between CLK and SCK (i.e. quadrature) which are used in the frequency detector/comparator (figure 1));

a frequency detector (fig. 4: element 33: frequency detector: col. 8, lines 1-9);

a first low-pass filter (fig. 4: element 37: col. 8, lines 1-9););

a second low-pass filter (fig. 4: element 35: col. 8, lines 1-9);

a first charge pump (fig. 4: element 36) for inputting a coarse control input for the voltage controlled oscillator (fig. 4: elements 31 and 36: note examiner interprets the

input of the VCO coupled to the frequency error (obvious the output of the frequency detector) to be the coarse control input: col. 8, lines 1-15) using a frequency error signal produced by the frequency detector and coupled to the first low-pass filter (fig. 4: element 35: col. 8, lines 1-15);

a second charge pump (fig. 4: element 34: col. 8, lines 1-9); and

a further phase detector (fig. 4: element 32: col. 8, lines 1-9);

wherein a fine control input is controlled by a signal provided by the further phase detector coupled to the second charge pump coupled to the second low-pass filter (fig. 4: elements 31, 32, 34, and 35: col. 8, lines 1-15: note examiner interprets the input of the VCO coupled to the phase error (obvious the output of the phase detector) to be the fine control input: col. 8, lines 1-15).

One of orindary skill in the art at the time of the invention would clearly recognize the benefits of replacing the frequency detector within the PLL circuit structure disclosed by Tamaki with the differential quadricorrelator (frequency detector for differential signal) disclosed by Moser in view Sudjian since the PLL circuit structure disclosed by Tamaki has the advantages of avoiding/preventing the trouble of harmonic lock by performing frequency detection without an external reference signal (col. 4, lines 3-8). Therefore it would have been obvious to one of orindary skill in the art at the time of the invention to replace the frequency detector within the PLL circuit structure disclosed by Tamaki with the differential quadricorrelator (frequency detector for differential signal) disclosed by Moser in view Sudjian, since the PLL circuit structure disclosed by Tamaki has the advantages of avoiding/preventing the trouble of harmonic lock by performing frequency

detection without an external reference signal (Tamaki: col. 1, lines 5-11 and col. 4, lines 3-8: note the external reference clock is describe by figure 5).

Furthermore, a second input to the adder is not claimed. Thus in the case where the second input signal to the adder is zero, the limitation of the adder (and its coupling between the coarse VCO input and the first low-pass filter) does not define a patentably distinct invention over Tamaki since both inventions as a whole are directed to a PLL structure in which the VCO has a coarse and fine inputs which are respectively coupled to a frequency detector and a phase detector. Therefore, the adder and the adder's coupling would have been a matter of obvious design choice to one of ordinary skill in the art.

Allowable Subject Matter

8. Claims 1-2, 5-6, and 8-9 are allowed.

9. The following is an examiner's statement of reasons for allowance:

(1) With respect to claims 1-2 and 5-6, the present invention comprises a Phase Locked Loop (PLL), for synchronization of a clock signal with an incoming data signal, comprising a frequency detector including an unbalanced quadricorrelator, the quadricorrelator including a first multiplexer, a second multiplexer, and double edge clocked bi-stable circuits, supplied by incoming mutually quadrature phase shifted signals and coupled to the first multiplexer and to the second multiplexer, the first and second multiplexers controlled by a signal having a same bit-rate as the incoming signal; a first phase detector that includes a D flip flop that receives, as a data input, a first signal pair provided by the first multiplexer and that is clocked by a second signal

pair provided by the second multiplexer; a first transistor pair receiving the second signal pair on respective gates for determining a state ON or OFF of a current through the first transistor pair; and a second transistor pair biased by current through the first transistor pair and receiving the first signal pair and generating an output signal indicative for a frequency error between the incoming data signal and the clock signal. The closest prior art, Moser (United States Patent No. 6,853,696), shows a similar system which also includes a phase locked loop comprising a frequency detector including an unbalanced quadricorrelator utilizing D flip-flops and multiplexers. However Moser fails to disclose the frequency detector including unbalanced quadricorrelator as claimed, first phase detector as claimed, first transistor pair as claimed, and second transistor pair as claimed. The distinct features have been added to independent claim 1, therefore rendering claims 1-2 and 5-6 allowable.

(2) With respect to claim 8, the present invention comprises a Phase Locked Loop, for use with an incoming data comprising: a voltage controlled oscillator having a coarse control input and a fine control input and generating mutually quadrature phase-shifted signals; a first charge pump; a second charge pump; a first low-pass filter; a second low-pass filter; an adder; a quadricorrelator generating a frequency error signal inputted to the coarse control input of the voltage controlled oscillator via the first charge pump coupled to the first low-pass filter coupled to the adder, the quadricorrelator including a frequency detector including a first multiplexer, a second multiplexer, a first pair of double edge clocked bi-stable circuits coupled to the first multiplexer and a second pair

of double edge clocked bi-stable circuits coupled to the second multiplexer to provide a second signal pair, the first and second pairs of bi-stable circuits being supplied by the mutually quadrature phase shifted signals, the first and second multiplexers being controlled by a signal having a same bit-rate as the incoming signal and respectively providing a first signal pair and a second signal pair indicative for a phase difference between an incoming signal and the mutually quadrature phase shifted signals; a transistor pair; and a phase detector controlled by the first signal pair and the second signal pair, the phase detector including a D flip-flop receiving the first signal pair and being clocked by the second signal pair, the second signal pair being inputted to respective gates of the transistor pair for determining a state ON or OFF of a current through said transistor pair; and a second phase detector generating a phase error inputted to the fine control input of the voltage controlled oscillator via the second charge pump coupled to the second low-pass filter. The closest prior art, Moser (United States Patent No. 6,853,696), shows a similar system which also includes a phase locked loop comprising a frequency detector including an unbalanced quadricorrelator utilizing D flip-flops and multiplexers, local clock generator, a charge pump, loop filter, and phase detector. However Moser fails to disclose the frequency detector as claimed, phase detectors as claimed, the low-pass filters as claimed, and VCO as claimed. The distinct features have been added to independent claim 8, therefore rendering claims 8 and 9 allowable.

10. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES M. PEREZ whose telephone number is (571)270-3231. The examiner can normally be reached on Monday through Friday: 9am to 5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/James M Perez/
Examiner, Art Unit 2611
2/16/2010
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611